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PATENTS
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicant	: Glen J. Leedy	
Application No.	: 10/614,067	Confirmation No. : 8117
Filed	: July 3, 2003	
For	: THREE DIMENSIONAL STRUCTURE INTEGRATED CIRCUIT	
Group Art Unit	: 2822	
Examiner	: Pamela E. Perkins	

New York, New York 10020
November 14, 2006

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Sir:

The above-identified patent application was allowed on October 10, 2006. The Notice of Allowability included a Statement of Reasons for Allowance.

While applicant appreciates the allowance of this application, applicant notes that the Statement of Reasons for Allowance includes general characterizations for groups of claims that include features not actually included in the individual claims. A particular claim only includes those features explicitly recited in that particular claim.

In the Statement of Reasons for Allowance, the Examiner stated:

> "Referring to claims 88, 97 and 101, prior art does not anticipate, teach, or suggest a plurality of monolithic substrates having integrated circuits formed thereon and stacked in layers such that each layer comprises only one of the substrates, wherein at least one of the plurality of substrates is a substantially flexible substrate, and wherein a major portion of the monolithic substrate is removed." (Notice of Allowance, page 2)

However, applicant notes that claims 97 and 101 do not include some of the features indicated by the Examiner. The Examiner's statement is merely a characterization of features included in claim 88 and does not address the claims individually. The statement thereby incorrectly applies particular features of claim 88 to claims 97 and 101.

More particularly, claim 97 is allowable because none of the prior art shows or suggests:

> 97. An integrated circuit structure comprising:
>
> a first substrate having a first surface; and
>
> a second substrate bonded to the first surface of the first substrate to form conductive paths between the first substrate and the second substrate wherein the second substrate is a substantially flexible monolithic monocrystalline semiconductor substrate having active circuitry formed thereon, wherein no other substrates are bonded to the first surface, and wherein a major portion of the second substantially flexible monolithic monocrystalline semiconductor substrate is removed.

Additionally, claim 101 is allowable because none of the prior art shows or suggests:

> 101. A stacked integrated circuit comprising:
>
> a plurality of integrated circuit substrates having formed on corresponding surfaces

thereof complementary patterns of a material bondable using thermal diffusion bonding, wherein at least one of the plurality of substrates is a substantially flexible monolithic integrated circuit substrate, and wherein a major portion of the at least one substantially flexible monolithic integrated circuit substrate is removed; and

a thermal diffusion bonded region between the complementary patterns.

The Statement of Reasons for Allowance additionally stated:

"Referring to claims 128, 146 and 156, prior art does not anticipate, teach, or suggest wherein at least one substrate to the first and second substrates has reconfiguration circuitry." (Notice of Allowance, page 3)

However, applicant notes that claims 146 and 156 do not include some of the features indicated by the Examiner. The Examiner's statement is merely a characterization of features included in claim 128 and does not address the claims individually. The statement thereby incorrectly applies particular features of claim 128 to claims 146 and 156.

More particularly, claim 146 is allowable because none of the prior art shows or suggests:

146. (Previously presented) An integrated circuit structure comprising:

a plurality of semiconductor dice, each die having an integrated circuit formed thereon, said dice being stacked in layers, wherein at least one of the plurality of dice is substantially flexible, and wherein at least one of the plurality of dice has at least one of polycrystalline active circuitry formed thereon, reconfiguration circuitry formed thereon, and passive circuitry formed thereon; and

between adjacent dice, a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice.

Additionally, claim 156 is allowable because none of the prior art shows or suggests:

> 156. (Previously presented) An integrated circuit structure comprising:
>
> a substrate having a first surface; and
>
> a semiconductor die having an integrated circuit formed thereon bonded to the first surface of the substrate with conductive paths between the substrate and the die wherein the die is substantially flexible, wherein the semiconductor die is attached to the first surface of the substrate by one or more bonds including one bond located other than at the edges of the semiconductor die, and wherein at least one of the substrate and die has at least one of polycrystalline active circuitry formed thereon, reconfiguration circuitry formed thereon, and passive circuitry formed thereon.

In light of the foregoing, applicant respectfully requests that the Examiner issue a revised Statement of Reasons for Allowance setting forth the reasons for allowance of each respective one of claims 97, 101, 146 and 156.

Respectfully submitted,

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